Q1. (20pts) Please explain the following terms briefly.
   a) channel length modulation
   b) body effect
   c) beta ratio effect
   d) antenna rules
   e) Elmore delay model
   f) Logical effort
   g) Fringing effect on capacitance
   h) Process corners
   i) Latchup
   j) Monte Carlo simulation

Q2. The operation of a CMOS inverter can be divided into 5 regions as shown into 5 regions.
   a) Refer to Table 1, derive analytic expressions for $V_{out}$ as a function of $V_{in}$ for regions B and D of the transfer function. Let $|V_p| = V_{tn}$ and $\beta_p = \beta_n$ (5pts)
   b) Calculate its noise margin for $V_{DD} = 1.2V$ and $V_{in} = |V_p| = 0.4V$ (5pts)

<table>
<thead>
<tr>
<th>Region</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>$0 \leq V_{in} &lt; V_m$</td>
</tr>
<tr>
<td>B</td>
<td>$V_m \leq V_{in} &lt; V_{DD}/2$</td>
</tr>
<tr>
<td>C</td>
<td>$V_{in} = V_{DD}/2$</td>
</tr>
<tr>
<td>D</td>
<td>$V_{DD}/2 &lt; V_{in} \leq V_{DD} -</td>
</tr>
<tr>
<td>E</td>
<td>$V_{in} &gt; V_{DD} -</td>
</tr>
</tbody>
</table>

Q3. Consider the two designs for a 2-input AND gate shown in Figure 1.
   a) Please calculate the path electrical effort $H$, logical effort $G$, path effort $F$, and path delay $D$ of each design.(5pts)
   b) What are the input capacitances $x$ and $y$ required to achieve such path delays? (5pts)
Q4. For the clock buffer shown in Figure 2, assume the maximum input capacitance is 150fF. Both true and complementary outputs must drive loads of 400pF.
   a) Please compute the input capacitance of each inverter to minimize the worst case delay from input to either output (5pts)
   b) Assume the inverter parasitic delay is 1, what is this delay in μs? (5pts)

![Figure 2.](image)

Q5. a) Please explain setup time failure. (5pts)
   b) Can setup time failure be solved by increasing the clock period? (5pts)
   c) Can hold time failure be solved by increasing the clock period? (5pts)

Q6. a) Sketch a LO-skew 3-input NOR gate. (5 pts)
   b) Label the transistor widths. (5 pts)
   c) What is the logical effort of this gate on its critical transition? (5 pts)

Q7. Sketch a dynamic unfooted 3-input NAND gate. (10 pts)

Q8. For latches: contamination delay = 40ps, hold time = 35ps, setup time = 30ps, clk-to-Q delay = 55ps, D-to-Q delay = 45ps, determine the maximum logic propagation delay available within a 500ps clock cycle if the sequencing style is two-phase transparent latches. Assume there is zero clock skew and no time borrowing takes place. (10 pts)