PART - I (50%)

1. Which of the following bit patterns represents the value -5 in two’s complement notation?
   (1) 00011010  (2) 11111011  (3) 00000101  (4) 11111011  (5) none of above

2. What is the output of the circuit below?

   Input Pattern
   1  0  1
   0  →  →  →  Output

3. Which of the following is not an activity performed entirely within a CPU?
   (1) Fetch instructions
   (2) Perform Boolean operations
   (3) Perform arithmetic operations
   (4) Move data between registers
   (5) none of them

4. Which of the following connects existing networks to form an internet?
   (1) Bridge  (2) Router  (3) Switch  (4) Repeater  (5) none of them

5. Which layer of the TCP/IP hierarchy decides the direction in which message segments are transferred across the Internet?
   (1) Application  (2) Transport  (3) Network  (4) Link  (5) none of them
6. The binary search algorithm is an example of an algorithm in which of the following classes?
(1) $\Theta(\lg n)$ (2) $\Theta(n)$ (3) $\Theta(n \lg n)$ (4) $\Theta(n^2)$ (5) none of them

7. Which of the following is not constructed by a typical compiler?
(1) Source code (2) Symbol table (3) Parse tree (4) Object program (5) all of them are constructed by a compiler

8. If a class diagram indicates a one-to-one relationship between class X and class Y, then
(1) there will be only one object in the system of “type” X.
(2) each object of “type” X will be associated with only one object of “type” Y.
(3) there will be exactly one object of “type” X and exactly one object of “type” Y.
(4) an object of “type” Y cannot occur without first constructing an object of “type” X.
(5) none of above.

9. What sequence of nodes from the tree would be printed if the following recursive procedure were applied to it? (The procedure uses a global stack called Stack that is assumed to begin empty.) Assume A=1, B=2, C=3, D=4, E=5, F=6, and G=7. Report the multiplication result of the output nodes. For example, if the out nodes are A, B, E, you should report the result of $A \times B \times E$ which is equivalent to $1 \times 2 \times 5 = 10$.
procedure printTree (Tree)
if (Tree is not empty)
    then (push the current node on Stack;
        apply the procedure printTree to the right subtree of Tree)
if (Stack is not empty)
    then (pop an entry from Stack and print that node)

(1) 21  (2) 18  (3) 10  (4) 8  (5) none of them

10. Which of the following questions has not yet been answered by researchers?
(1) Is P contained in NP?
(2) Is NP contained in P?
(3) Are all the problems in NP solvable?
(4) Are all the problems in P solvable?
(5) none of them
PART 2

1. Please fill the following blanks in **English** (10%).

   (a) The use of registers for the page table is satisfactory if the page table is reasonably small (for example, 256 entries). Most contemporary computers, however, allow the page table to be very large (for example, 1 million entries). For these machines, the use of fast registers to implement the page table is not feasible. Rather, the page table is kept in main memory, and a (1) register points to the page table. Changing page tables requires changing only this one register, substantially reducing context-switch time. Nevertheless, the problem with this approach is the time required to access a user memory location. The standard solution to this problem is to use a special, small, fast-lookup hardware cache, called a (2). In addition, some of this cache stores (3) in each entry. A (4) uniquely identifies each process and is used to provide address-space protection for that process. If the (2) does not support separate (3), then every time a new page table is selected (for instance, with each context switch), the TLB must be (5) to ensure that the next executing process does not use the wrong translation information.

   (b) To handle bad blocks, more sophisticated disks, such as the SCSI disks used in high-end PCs and most workstations and servers, are smarter about bad-block recovery. The controller maintains a list of bad blocks on the disk. The list is initialized during the low-level formatting at the factory and is updated over the life of the disk. Low-level formatting also sets aside spare sectors not visible to the operating system. The controller can be told to replace each bad sector logically with one of the spare sectors. This scheme is know as (5).

2. The process control block usually maintains many pieces of information that are associated with a specific process. For example, it might contain field to store the values of CPU registers. However, the CPU registers are hardware and are inside the CPU. Why the operating systems add the CPU register values into the PCB? (3 pt)

3. The program shown in the following uses the Pthread API. What would be the output from the program at LINE C and LINE P? (6 pt)

```c
#include <pthread.h>
#include <stdio.h>

int value = 0;
void *runner(void *param);

int main(int argc, char *argv[])
{
    int pid;
    pthread_t tid;
    pthread_attr_t attr;

    pid = fork();
    if (pid == 0) {
        pthread_attr_init(&attr);
        pthread_create(&tid, &attr, runner, NULL);
        pthread_join(tid, NULL);
        printf("value = %d",
```
void *runner(void *param) {
    value = 5;
    pthread_exit(0);
}

4. Following shows a C program using POSIX APIs

#include <stdio.h>
#include <sys/shm.h>
#include <sys/stat.h>

int main() {
    int segment_id;
    char *buffer;
    const int size = 4096;

    segment_id = shmget(IPC_PRIVATE, size, S_IRUSR|S_IWUSR);
    buffer = (char *) shmat(segment_id, NULL, 0);
    sprintf(buffer, "Hi there!");
    printf("%s\n", buffer);
    shmdt(buffer);
    shmct1(segment_id, IPC_RMID, NULL);
    return 0;
}

(a) Which IPC (Inter-Process Communication) scheme is adopted in the above program? (2 pt)
(b) What is the purpose of shmget() function? (2 pt)
(c) What is the purpose of shmat() function. (2 pt)

5. Our favorite program runs in 10 seconds on computer A, which has a 2GHz clock. We are trying to help a computer designer build a computer, B, which will run this program in 6 seconds. The designer has determined that a substantial increase in the clock rate is possible, but his increase will affect the rest of the CPU design, causing computer B to require 1.2 times as many clock cycles as computer A for this program. What clock rate should we tell the designer to target? (Please show your calculation step by step) (4 pt)
Figure 1: The basic implementation of the MIPS subset, including the necessary multiplexors and control lines. The two adders are termed “branch add” and “normal add” respectively for differentiation.

6. Different instructions utilize different hardware blocks in the basic single-cycle implementation. The next three problems in this exercise refer to the following instructions: (12 pt)

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Interpretation</th>
</tr>
</thead>
<tbody>
<tr>
<td>a. add Rd, Rs, Rt</td>
<td>Reg[Rd] = Reg[Rs] + Reg[Rt]</td>
</tr>
<tr>
<td>b. lw Rt, Offs(Rs)</td>
<td>Reg[Rt] = Mem[Reg[Rs] + offs]</td>
</tr>
</tbody>
</table>

(a) What are the values of control signals generated by the control in Figure 1 for the above two instructions? (Please answer the questions using the following table format).

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(b) Which resources (blocks) perform a useful function for these two instructions?
(c) (i) Which resources (blocks) produce outputs, but their outputs are not used for these two instructions? (ii) Which resources produce no output for these two instructions?

7. Assume there are three small caches, each consisting of four one-work blocks. Given the following sequence of block addresses: 0, 8, 0, 6, 8, find the number of misses for the following three kinds of cache organizations. Assume using the least recently used replacement scheme. (a) Fully associative cache, (b) Two-way set-associative cache, (c) Direct-mapped cache (Please show your calculation step by step). (9 pt)