Q1. (10pts) A 3-input majority logic is true if at least two of the inputs are true. A minority logic is its complement. 
Design a 3-input CMOS minority gate using a single stage of logic 
   a) Sketch a transistor level design 
   b) Find a common Euler path between N-block and P-block 
   c) Sketch a stick diagram according to the Euler path 

Q2. (12pts) As shown in Fig. 1, if all nMOS (pMOS) transistors have identical trans-conductance $\beta_n$ ($\beta_p$), 
   a) Refer to Table 1, please fill in the equivalent trans-conductance ratio of N-block to P-block, using $\beta_n / \beta_p$ as the measurement unit 
   b) For the three transitions (A,B,C), please label the corresponding curves in Fig. 2.

<table>
<thead>
<tr>
<th>transition</th>
<th>Initial (x,y,z)</th>
<th>Final (x,y,z)</th>
<th>N-block to P-block transconductance ratio</th>
<th>Corresponding Transfer curve</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>(0, 0, 0)</td>
<td>(1, 1, 1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>(1, 0, 1)</td>
<td>(1, 0, 0)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>(1, 1, 0)</td>
<td>(1, 0, 0)</td>
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</table>

Q3. (10pts) Consider a process with pMOS transistors three times the effective resistance as nMOS transistors. 
Calculate the logical efforts of a 2-input NAND gate and a 2-input NOR gate if they are designed with equal rising and falling delay.
Q4. (10pts) Sketch 3-input XOR functions using each of the following circuit techniques
   a) Pseudo NMOS
   b) Dual rail domino
   c) CPL

Q5. (8pts) Refer to Figure 3
   a) Please draw the schematic of the layout
   b) What is the circuit design for?

Q6. (15pts) Figure 4 shows a 16-bit Ladner-Fischer adder. Please sketch a diagram of the group PG tree for a 32-bit Ladner-Fischer adder. Buffer can be ignored.

Q7. (10pts) What are the functions/requirements for packages?

Q8. (10pts) For Flip-flops: Contamination delay = 35ps, hold time = 30ps, setup time = 60ps, clk-to-Q delay = 50ps, determine the maximum logic propagation delay available within a 600ps clock cycle if the sequencing style is Flip-flops. Assume there is zero clock skew and no time borrowing takes place.

Q9. (15pts) Please compare the full custom design, the cell-based design, and the gate array design in terms of cost, speed, etc.